

Exhibit 6



**UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.**

In the Matter of

**CERTAIN MEMORY MODULES AND
COMPONENTS THEREOF**

Investigation No. 337-TA-1089

COMMISSION OPINION

The Commission has determined that there has been no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, with respect to U.S. Patent Nos. 9,606,907 (“the ’907 patent”) and 9,535,623 (“the ’623 patent”) on review of the Final Initial Determination (“ID”) of the presiding administrative law judge (“ALJ”). This opinion sets forth the Commission’s reasoning in support of that determination.

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation on December 4, 2017, based on a complaint filed by Netlist, Inc. of Irvine, California (“Netlist”). 82 Fed. Reg. 57290-91. The complaint alleged violations of section 337 in the importation into the United States, the sale for importation, and the sale after importation within the United States of certain memory modules and components thereof by reason of infringement of one or more of claims 1-8, 10, 12, 14-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the ’907 patent and claims 1-5, 7-15, 17-25, 27, and 29 of the ’623 patent. *Id.* at 57291. The notice of investigation named as respondents SK hynix Inc. of the Republic of Korea; SK hynix America Inc. of San Jose, California; and SK hynix memory solutions Inc. of San Jose, California (collectively, “SK hynix”). *Id.* The Office of Unfair Import Investigations (“OUII”) is a party to the investigation. *Id.*

The Commission subsequently terminated the investigation with respect to certain claims based on Netlist's withdrawal of those allegations. Specifically, the Commission terminated the investigation with respect to claims 16-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the '907 patent and claims 12-15, 17-25, 27, and 29 of the '623 patent based on Netlist's partial withdrawal of its complaint. *See* Order. No. 12 (Mar. 19, 2018), *not reviewed*, Notice (Apr. 5, 2019); Order. No. 19 (Sept. 25, 2018), *not reviewed*, Notice (Oct. 15, 2018); Order. No. 27 (Dec. 6, 2018), *not reviewed*, Notice (Dec. 21, 2018). Accordingly, at the time of the Final ID, the remaining asserted claims were claims 1-8, 10, 12, 14, and 15 of the '907 patent and claims 1-5 and 7-11 of the '623 patent.

On October 19, 2019, the ALJ issued the Final ID finding a violation of section 337 with respect to claims 6 and 12 of the '907 patent. Final ID at 164-65. The ALJ found that Netlist showed that SK hynix infringed claims 1-8, 10, 12, 14, and 15 of the '907 patent, but failed to show that SK hynix infringed any claim of the '623 patent. *Id.* The ALJ also found that SK hynix showed that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious, but failed to show the invalidity of claims 6 and 12. *Id.* at 165. Finally, the ALJ found that Netlist satisfied the domestic industry requirement with respect to the '907 patent, but did not satisfy the domestic industry requirement with respect to the '623 patent.

On October 29, 2019, the Commission sought submissions from the public regarding the public interest raised by the ALJ's recommend limited exclusion order. 84 Fed. Reg. 57884. The Commission received submissions on the public interest from SK hynix; Netlist; the U.S. Federal Trade Commission; Congressman Ted Budd; Congressman John Carter; Congresswoman Anna G. Eshoo; Congressman Henry C. Johnson; Congresswoman Katie Porter; Ericsson, Inc.; Dell, Inc.; Hewlett Packard Enterprise; JEDEC; ACT The App

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Association and several individuals—Cameron Bopp, James Laipple, K. Elbarjaj, Franklin P. Stone, and Stuart Douglass.

On November 4, 2019, SK hynix¹ and OUII² filed petitions for review. SK hynix petitioned for review of several of the ALJ’s findings on claim construction, infringement, the domestic industry, and invalidity with respect to the ’907 patent, and also challenged several of the ALJ’s rulings on its Reasonable and Non-Discriminatory (“RAND”) defenses and estoppel due to *inter partes* review (“IPR”) proceedings at the Patent Trial and Appeal Board (“PTAB”) regarding the ’907 patent. OUII petitioned for review of several of the ALJ’s findings on claim construction, infringement, the domestic industry, and invalidity with respect to the ’907 patent. Also on November 4th, Netlist filed a contingent petition for review on several invalidity issues and the ALJ’s recommendation on a cease and desist order with respect to the ’907 patent.³ No one petitioned for review with respect to the ’623 patent findings. On November 12, 2019, the parties filed responses to each other’s petitions.⁴

On January 31, 2020, the Commission determined to review the following issues: (1) the construction of the limitation “receive” in the asserted claims of the ’907 patent, as well as related issues of infringement and invalidity; (2) the construction of the limitation “produce first module control signals and second module control signals in response to the set of input address

¹ Respondents’ Petition for Review (Nov. 4, 2019) (“SK hynix Pet.”).

² The Office of Unfair Import Investigation’s Petition for Review in Part of the Final Initial Determination (Nov. 4, 2019) (“OUII Pet.”).

³ Complainant Netlist, Inc.’s Contingent Petition for Review of the Initial Determination (Nov. 4, 2019) (“Netlist Pet.”).

⁴ Complainant Netlist, Inc.’s Omnibus Response to Respondents’ and Staff’s Petitions for Review (Nov. 12, 2019) (“Netlist Resp.”); Respondents’ Combined Response to (1) Petition for Review by the Office of Unfair Import Investigations and (2) Contingent Petition for Review by Complainant (Nov. 12, 2019) (“SK hynix Resp.”); Response of the Office of Unfair Import Investigations to the Private Parties’ Petitions for Review of the Initial Determination on Violation of Section 337 (Nov. 12, 2019) (“OUII Resp.”).

and control signals” in the asserted claims of the ’907 patent, as well as related issues of infringement and invalidity; (3) the domestic industry requirement with respect to both of the ’623 and ’907 patents; and (4) the findings with respect to both of the ’623 and ’907 patents regarding whether SK hynix showed that Netlist violated its obligations, if any, to offer a license on reasonable and non-discriminatory terms. The Commission did not determine to review the ALJ’s conclusion that there was no violation of section 337 with respect to the ’623 patent based on a lack of infringement. The Commission also sought briefing on certain issues under review and on remedy, the public interest, and bonding.

On February 14, 2020, the Commission received initial submissions from Netlist, SK hynix, and OUII.⁵ The Commission also received a submission on the public interest from third-party Hewlett Packard Enterprise Company. On February 24, 2020, the Commission received reply submissions from Netlist, SK hynix, and OUII.⁶

B. The ’907 Patent

The ’907 patent is entitled “Memory Module with Distributed Data Buffers and Method of Operation” and claims priority as a continuation of an application filed on April 15, 2010 and as a continuation-in-part of an application that was filed on July 16, 2009. JX-2001 (’907 patent). The patent generally describes a memory module in which a data buffer circuit reduces the overall electrical load by transmitting command data only to the selected memory device while not transmitting the command data to non-selected devices. The only independent claim at issue, claim 1, reads as follows, with the terms at issue highlighted in bold:

⁵ These documents will be referred to as “Netlist Init. Sub.,” “SK hynix Init. Sub.,” and “OUII Init. Sub.,” respectively.

⁶ These documents will be referred to as “Netlist Rep. Sub.,” “SK hynix Rep. Sub.,” and “OUII Rep. Sub.,” respectively.

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1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and $N=M \times n$, comprising:

a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to **produce first module control signals and second module control signals in response to the set of input address and control signals;**

a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while **the second memory devices do not output or receive any data associated with the memory read or write command;**

M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and

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between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

JX-2001 ('907 patent) at 19:2-58.

C. The Accused Products

Netlist accused many models of SK hynix's JEDEC-compliant Double Data Rate 4 ("DDR4") Load-Reduced Dual In-Line Memory Module ("LRDIMM") products of infringing the '907 patent. Final ID at 7-8. The specific accused models are listed in a table on pages 7-8 of the Final ID. *Id.*

D. The Domestic Industry Products

The asserted domestic industry articles are Netlist's 16 GC 2Rx4 DDR HV-LRDIMM and 32GB 2Rx4 DDR HV-LRDIMM. Final ID at 10. These products are specific model numbers of Netlist's Field Programmable Gate Array ("FPGA") HybriDIMM product. *Id.* at 139. Netlist has since transitioned to its Application-Specific Integrated Circuit ("ASIC") HybriDIMM product, but expressly stated that it was not relying upon that product for the domestic industry. *Id.* at 139 n.13.

II. STANDARD

With respect to the issues under review, "the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge." 19 C.F.R. § 210.45(c). The Commission also "may take no position on specific issues or portions of the initial determination," and "may make any finding or

conclusions that in its judgment are proper based on the record in the proceeding.” *Id.*

III. DISCUSSION OF THE ISSUES ON REVIEW

The Commission determines to make the findings, conclusions, and supporting analysis set forth below. Any findings, conclusions, and supporting analysis in the ID that are under review and are not inconsistent with the Commission’s analysis and conclusions below are hereby affirmed and adopted.

A. The “Receive” Limitation in the Asserted Claims of the ’907 Patent

For the reasons set forth below, the Commission determines to construe “receive” according to its plain and ordinary meaning, and thus finds that a circuit element “receives” a signal or data when the signal or data reaches a circuit element’s input. Under that construction, the Commission finds that Netlist failed to establish infringement or the technical prong of the domestic industry requirement for any asserted claim of the ’907 patent, and affirms under modified reasoning the ALJ’s finding that claims 1-5, 7, 8, 10, 14, and 15 of the ’907 patent are invalid as obvious.

1. Claim Construction

a. Overview

The issue under review concerns the construction of the term “receive.” The term “receive” appears several times in the asserted claims, but most notably in the following limitation of claim 1:

a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or **receive** each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or **receive** any data associated with the memory read or write command

’907 patent, claim 1 (emphasis added). Claim 1 uses the term “receive” similarly elsewhere—“a

module control circuit configured to receive a set of input address and control signals . . .” and “M buffer circuits each configured to receive the second module control signals . . .” *Id.*

During claim construction, the parties disputed the construction of the term “output or receive . . . data” / “do not output or receive any data.” Netlist contended that the term should be construed as “transmit or acquire data” / “do not transmit or acquire data.” SK hynix argued that the term should be construed as its plain and ordinary meaning, but with a complex understanding as to what the plain and ordinary meaning is. OUII argued that the term should be construed as “non-selected devices do not receive any data or send any data associated with the memory controller read/write command.”

Judge Pender, who presided over the claim construction hearing, acknowledged that the ’907 patent used “receive” consistent with its plain and ordinary meaning. Order No. 17, at 32 (Aug. 24, 2018). He noted that SK hynix’s claim construction was persuasive because “it revolves around a plain and ordinary meaning of ‘receive’—a circuit element ‘receives’ a signal when that signal reaches one of the circuit element’s inputs,” and because it is also consistent with the specification. *Id.* The ALJ further explained that “the ’907 patent does not expressly define what is meant by ‘output’ or ‘receive’” and acknowledged that the patent uses “receive” in a variety of contexts, which “support[s] the idea that the ’907 patent uses ‘output’ and ‘receive’ according to general, plain and ordinary meanings.” *Id.*

The ALJ, however, ultimately adopted Netlist’s proposed construction of “output or receive” as “transmit or acquire,” “even though I find it may not match the plain and ordinary meaning of ‘output’ and ‘receive.’” *Id.* at 25. Generally, the ALJ favored Netlist’s argument that the claims covered a “straight line” arrangement (in which the first and second memory devices share data lines from their respective buffer circuits) over SK hynix’s argument that the

claims required a “fork-in-the-road” arrangement (in which the first and second memory devices have separate data lines from their respective buffer circuits). *Id.* at 25. The ALJ relied upon unasserted and unargued claim 30, which required the limitation “first memory devices responding to the first output address and control signals by receiving each N-bit wide data signal associated with the first write command,” and found that the “by receiving” language implied that “receiving” is an action performed by the memory devices rather than the result of an external act. *Id.* at 27.

Chief Judge Bullock, who took over the investigation and presided over the hearing and issued the Final ID, further explained the meaning of “receive” in the Final ID. He stated that “[t]he parties are effectively in agreement that Order No. 17 construed ‘receive’ as ‘acquire,’ and that ‘acquire’ was understood in that order as meaning ‘the first stage of a write operation.’” Final ID at 92. Accordingly, between the findings of Judge Pender and Chief Judge Bullock, the term “receive” has been construed to mean “a first stage of a write operation.”

b. Petition and Response

In its petition for review, SK hynix argued that claim terms are generally given their plain and ordinary meaning, and thus the ALJ erred by failing to give “receive” its plain and ordinary meaning that was expressly set forth in Order No. 17—“a circuit element ‘receives’ a signal when that signal reaches one of the circuit element’s inputs.” SK hynix Pet. at 12. SK hynix argued that the plain and ordinary meaning is consistent with the specification, and that the ALJ’s reliance on the unasserted and unbriefed claim 30 does not apply to the claimed invention of the asserted claims. *Id.* at 12-18.

Netlist argued that SK hynix never previously argued to construe the term “receive” on its own, and therefore waived the above argument by failing to present it to the ALJ. Netlist

Resp. at 7-11, 17. According to Netlist, Judge Pender properly construed “receive” to mean “acquire” in the context of the ’907 patent, *id.* at 11-14, and Chief Judge Bullock properly applied the construction to find infringement, *id.* at 14-15.

OUII argued that the ALJ’s claim construction should not be reviewed. OUII Pet. at 29-35. While OUII believed that the ’907 patent is limited to a selective buffer circuit based on repeated disclaimers made during prosecution, OUII believed that concept can be incorporated by reviewing the construction of “buffer circuit” only. *Id.*

c. Analysis

While the parties’ claim construction arguments focused on the contrast of terms not found in the patent (*i.e.*, “straight line” versus “fork-in-the-road”), the Commission finds that the parties contested whether this limitation should be given its plain and ordinary meaning. In claim construction, “the words of a claim are generally given their ordinary and customary meaning.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). The exceptions are when “the patentee sets out a definition and acts as his own lexicographer” or when “the patentee disavows the full scope of a claim term.” *Thorner v. Sony Comput. Entertainment America LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Here, as discussed above, Judge Pender found that the patentee did not define “receive” and that the plain and ordinary meaning of “receive” in the context of the ’907 patent is that “a circuit element ‘receives’ a signal when that signal reaches one of the circuit element’s inputs.” Order No. 17 at 32. No party disputed Judge Pender’s characterization of the plain and ordinary meaning of “receive.” Accordingly, the Commission has determined to adopt Judge Pender’s recitation of the plain and ordinary meaning of “receive” and construe “receive” to occur when a signal or data reaches a circuit element’s input.

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Netlist argues that “receive” should be construed as “acquire” based on the context of the ’907 patent and the skill in the art, but Netlist fails to explain why the specification or skill in the art would support construing “receive” as “acquire.” *See* Netlist Resp. at 11-14. As the ALJ noted, the specification does not give any special meaning to “receive,” and at times, the specification uses “receive” in exactly the plain and ordinary meaning described by Judge Pender. *See* ’907 Patent at 16:3-21 (describing “control logic circuit 502 receives, for example, an ‘enable A’ signal . . .” and “data signals . . . are received at the first or second terminals Y1, Y2 . . .”). Moreover, claim 1 recites “receive” four times, and it would be inconsistent to construe two instances of “receive” to mean “acquire” and the other two instances to mean something else. *See, e.g., Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001) (“[A] claim term should be construed consistently with its appearance in other places in the same claim or in other claims of the same patent.”).

Moreover, interpreting “receive” to have its plain and ordinary definition is consistent with the specification of the ’907 patent. The specification explains that, under prior art systems, a memory controller communicated read and write commands to all memory devices even though each command was intended for only one selected memory device. JX-2001 (’907 Patent) at 4:56-61; 5:7-13. Under these prior art systems, adding more memory devices to increase memory space required exponentially more command signals, which in turn caused heavy loads on the system that reduced speed, increased heat dissipation, caused signal propagation delay, necessitated asynchronous behavior, and created a need for extensive modification. *Id.* at 4:7-35; 5:14-34; 6:33-55; 7:6-34. The ’907 patent solved that problem through “load-reduced memory modules” that selectively send commands only to the selected

memory device while sending no commands to nonselected memory devices.⁷ In other words, in the described invention of the '907 patent, the system does not send commands to nonselected memory devices, so the nonselected memory devices never “receive” a signal or data on their circuit element’s inputs. The Commission’s construction of “receive” is therefore consistent with the specification.

Netlist’s proposed construction, on the other hand, would allow the system to send signals to both selected and nonselected memory devices as long as only the selected memory devices acted upon the command. Such a system, however, is akin to prior art systems and defeats the purpose of the invention of the '907 patent. Thus, the Commission declines to adopt Netlist’s construction of “receive” to mean “acquire.”

2. Infringement

The Commission finds that the accused products do not infringe any asserted claim of the '907 patent under the Commission’s ordinary language construction of “receive.” The asserted claims of the '907 patent require that the second, nonselected memory devices “do not output or receive any data associated with the memory read or write command.” The Final ID expressly found that data signals are received on the input pins of nonselected memory devices in the accused products:

The parties’ experts are in agreement that, during a write operation, the **incoming data signal lands on the input pins of all Accused Product memory devices regardless of whether they are selected (i.e., targeted) or not**—specifically, the input pin of a RCVRS

⁷ See *id.* at Abstract (referring to “enabling data communication” to one memory device and “isolating at least one second memory device”); *id.* at 2:47-59 and 8:32-44 (referring to “selectively allowing or inhibiting data transmission” among the memory devices); *id.* at 2:63-66 (referring to “circuits configured to selectively isolate the plurality of memory devices from the system memory controller”); *id.* at 11:27-12:5 (referring to a circuit that “selectively switches between two or more memory devices . . . so as to operatively couple at least one selected memory device . . . to the system memory controller”).

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circuit. (RX-3869C at Q/A 35, 68, 70; see CX-2003C at Q/A 388, 405)

Final ID at 92 (emphasis added). The Commission finds that the parties’ experts agreed that the alleged first and second memory devices are connected by a shared data bus, and thus the same read/write command data signals arrive at the input of both memory devices’ RCVRS circuit regardless of whether or not the memory device is selected. RX-3869C (Subramanian RWS) at Q/A 35, 68, 70; CX-2003C (Levitt DWS) at Q/A 401, 405, 408. Accordingly, because the evidence shows that the accused second memory devices do receive “data associated with the memory read or write command” on their circuit inputs, the Commission finds that the accused products do not infringe any of the asserted claims of the ’907 patent.

3. Domestic Industry

The technical prong of the domestic industry requirement involves an examination of “whether the industry produces articles covered by the asserted claims,” which “is essentially the same as that for infringement, *i.e.*, a comparison of the domestic products to the asserted claims.” *Alloc, Inc. v. Int’l Trade Comm’n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). Netlist asserts that the domestic industry must rise or fall with infringement; on that basis, the Commission finds that Netlist also failed to establish the technical prong of the domestic industry requirement as to the ’907 patent based on its failure to establish infringement. Additionally, for reasons discussed *infra*, the Commission finds that Netlist failed to provide sufficient evidence to satisfy the technical prong of the domestic industry requirement as to the ’907 patent.

4. Invalidity

The Commission finds that its construction of “receive” does not alter the Final ID’s conclusions that claims 1-5, 7, 8, 10, 14, and 15 of the ’907 patent are invalid as obvious. The ALJ found that these claims are invalid as obvious in light of the Quad Bank Memory (“QBM”)

prior art, which is a series of technical documents regarding the creation of two models of QBM products. Final ID at 116-29. With respect to the above “receive” limitation, the ALJ found that the limitation was satisfied based on Dr. Subramanian’s testimony. *Id.* at 121-23. Dr. Subramanian testified that “[a] Skilled Artisan would have also understood that it was obvious at the time to use isolation switches to disconnect inactive memory devices from a shared data bus,” and demonstrated that the QBM products used DDR1 SDRAM devices and that the relevant contemporary JEDEC standard described such use of isolation switches. RX-2006C (Subramanian DWS) at Q/A 1052-53. In other words, Dr. Subramanian testified that a person of ordinary skill in the art would have found it obvious to use isolation switches to ensure that the nonselected memory device did not receive data associated with read and write commands. Accordingly, the Commission’s modification to the construction of “receive” does not change the ALJ’s invalidity result.

B. The “Produce First Module Control Signals and Second Module Control Signals in Response to the Set of Input Address and Control Signals” Limitation in the Asserted Claims of the ’907 Patent

For the reasons set forth below, the Commission determines to construe the limitation “produce first module control signals and second module control signals in response to the set of input address and control signals” to require a response to at least one input address signal and at least one control signal, but without any requirement that any specific module control signal be based on both input address signals and control signals. Under that construction, the Commission finds that Netlist failed to establish infringement or the technical prong of the domestic industry requirement for any asserted claim of the ’907 patent, and affirms under modified reasoning the ALJ’s finding that claims 1-5, 7, 8, 10, 14, and 15 of the ’907 patent are invalid as obvious.

1. Claim Construction

a. Overview

All of the asserted claims of the '907 patent require the limitation “produce first module control signals and second module control signals in response to the set of input address and control signals.” In the Final ID, the ALJ found that the language “in response to the set of input address and control signals” is satisfied by a response to solely input address signals or by a response to solely control signals, as “a response to any one of those signals is a response to the set.” Final ID at 77.

b. Petition and Response

SK hynix argued in its petition that the plain language of the claim requires that each of the first module control signals and second module control signals must be based on both input address signals and control signals. SK hynix Pet. at 48-50. Netlist and OUII argued that the ALJ correctly construed the term. Netlist Resp. at 48-50; OUII Resp. at 22-23.

c. Analysis

When a claim involves commonly used terms, claim construction “involves little more than the application of the widely accepted meaning of commonly understood words.” *Philips*, 415 F.3d at 1314. Here, the language “set of input address and control signals” requires at least one input address signal and at least one control signal, because otherwise there is no “set” of input address and control signals. Consequently, the claim language that calls for the production of module control signals “in response to the set of input address and control signals” requires that those module control signals be produced in response to at least one input address signal and at least one control signal. This construction is consistent with the portions of the specification referring to the production of signals in response to both address and control signals. JX-2001 ('907 patent) at 15:59-64 (“address and control signals pass from the memory controller 420 to

the control circuit 430 which produces controls sent to the logical circuitry 502”); id. at 17:57-18:59 (same). Accordingly, the Commission finds that the limitation “produce first module control signals and second module control signals in response to the set of input address and control signals” requires producing first module control signals and second module control signals in response to at least one input address signal and at least one control signal.

Netlist contends that the limitation should be construed to be satisfied if the module control signals are produced in response to either input address signals or control signals. Netlist Resp. at 48-50. That interpretation, however, describes a response to address signals or a response to control signals, not a response to a “set” of address and control signals as required by the claims. The Commission rejects Netlist’s attempt to improperly rewrite the claim language.

SK hynix contends that the claim language requires that the first module control signals and the second module control signals each be based on both at least one address signal and at least one control signal. SK hynix Init. Sub. at 5-7. That construction is too restrictive. While the claim language does require that the production be in response to “a set of input address and control signals,” it does not require that any specific module control signal be based on both input address and control signals. Accordingly, while the Commission finds that this limitation requires a response to at least one input address signal and at least one control signal, the limitation does not require any specific module control signal be produced in response to both input address signals and control signals.

2. Infringement

Under the construction set forth above, the Commission finds that the accused products do not infringe any asserted claim of the ’907 patent. The asserted claims of the ’907 patent impose the following requirements on the “first module control signals:”

- “produce first module control signals and second module control signals in

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response to the set of input address and control signals;” and

- “in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command.”

In other words, while the “first module control signals” must be produced as set forth above, the “first module control signals” must also result in a response in which the first memory devices output or receive command signals while the second memory devices do not output or receive command signals.

Netlist, however, failed to show that any alleged “first module control signals” satisfy all of these limitations. First, although Netlist demonstrated that the accused products produce an inverted address signal in response to an input address signal, Netlist failed to show that the accused products respond to that inverted address signal by having first memory devices output or receive command signals while second memory devices do not. Second, although Netlist demonstrated that the accused products contain a component that has a mode that produces signals in response to control signals, Netlist failed to show that the accused products use that mode. Each of these points are discussed in more detail below.

First, although Netlist showed that the accused products invert certain address signals, Netlist never explained how the accused products use those inverted address signals, and thus failed to explain how the inverted address signals satisfied the remainder of the limitations of the claim. Netlist’s only alleged use of “input address signals” to create an alleged “first module control signals” is through a process called “address inversion.” CX-2003C (Levitt DWS) at Q/A 362-63. Netlist’s expert, Dr. Levitt, testified that the JEDEC RCD standard states that the RCD component receives an address signal, and then outputs the address signal to the A-Side DRAM device and outputs the inverted address signal to the B-Side DRAM device. *Id.* Inverting an

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address signal could be viewed as producing a signal in response to an input address signal.

The claims, however, are not satisfied by the mere production of “first module control signals” based on an input address signal. Rather, as shown above, the “first module control signals” must also result in a response in which the first memory devices output or receive command signals while the second memory devices do not. Netlist failed to present evidence on whether the accused products use the inverted address signal at all, let alone how the inverted address signal is used so that the first memory devices output or receive command signals while the second memory devices do not. Netlist Initial Post-Hearing Br. at 27, 35 (referring to address inversion for the production of “first module control signals,” but failing to address output inversion for later limitations); CX-2003C (Levitt DWS) at Q/A 362-63, 382 (same); Netlist Reply Post-Hearing Br. (containing no references to address inversion).

Thus, while Netlist may have explained how the inverted address signal is produced based on an input address signal, Netlist did not explain how a response to the inverted address signal causes the first memory devices to output or receive data while the second memory devices do not output or receive data. Because both features are required to constitute “first module control signals” within the meaning of the asserted claims, Netlist failed to demonstrate that address inversion satisfies the production of “first module control signals.” Accordingly, there is no evidence that any alleged “first module control signal” or “second module control signal” in the accused products is produced in response to input address signals, and thus there is no evidence that the limitation “to produce first module control signals and second module control signals in response to the set of input address and control signals” is satisfied.

Second, although Netlist identified a mode in a component of the accused products that allegedly produces “first module control signals” in response to control signals, Netlist failed to

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show that the accused products use that allegedly infringing mode. Other than the “address inversion” discussed above, the only alleged “set of input address and control signals” are control signals used in a certain mode described in the JEDEC Registering Clock Driver (“RCD”) specification—Encoded QuadCS Mode. CX-2003C (Levitt DWS) at Q/A 360-61. The RCD is a component of the accused products, and the JEDEC RCD standard explains that the RCD has “three basic modes of operation”—“Direct DualCS mode” (the “normal operating mode”), “Direct QuadCS mode,” and “Encoded QuadCS mode,” but Netlist only accuses the Encoded QuadCS mode of infringement. *Id.* at Q/A 360 (quoting CX-0417). Netlist, however, failed to analyze the accused products or the domestic industry products to determine whether those products utilize Encoded QuadCS Mode. Products do not necessarily use every feature of each of its components, so Netlist’s failure to show that the accused products use Encoded QuadCS mode has created an absence of record evidence on the issue. Accordingly, there is no record evidence that the accused products produce first module control signals in response to chip-select signals in Encoded QuadCS mode, and therefore none of Netlist’s alleged “first module control signals” satisfy the limitations of the claim.

Netlist contends that its apparatus claims cover what a device is rather than what a device does, and that it has no obligation to show that the accused products implement Encoded QuadCS mode. Netlist Rep. Sub. at 4. But the mere fact that a JEDEC standard requires that the RCD component be able to implement Encoded QuadCS mode does not necessarily mean that every device incorporating that RCD component will utilize Encoded QuadCS mode. Accordingly, while compliance with the JEDEC standard may suggest that the RCD component is capable of operating in three modes, including Encoded QuadCS mode, Netlist has not established that the accused products have been enabled to operate in each of the three modes,

and more particularly in the Encoded QuadCS mode. Therefore, Netlist has not shown that this claim limitation is met by the accused products.

3. Domestic Industry

Netlist contends that its domestic industry products practice the asserted claims for the same reasons that the accused products infringe. 2003C (Levitt DWS) at Q/A 290, 633. But Netlist also failed to establish that its domestic industry products use address inversion or Encoded QuadCS mode as required by the asserted claims of the '907 patent. CX-2003C at Q/A 637-38 (failing show that Encoded QuadCS mode is used in the accused products); *id.* at Q/A 639-40, 651-711 (describing address inversion, but failing to describe how address inversion is used in the remainder of the claim). Accordingly, Netlist failed to demonstrate the technical prong of the domestic industry requirement as to the '907 patent for the same reasons that it failed to demonstrate infringement. Additionally, for reasons discussed *infra*, the Commission finds that Netlist failed to provide sufficient evidence to satisfy the technical prong of the domestic industry requirement.

4. Invalidity

The Commission finds that its construction of “produce first module control signals and second module control signals in response to the set of input address and control signals” does not alter the Final ID’s conclusions that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious in light of the QBM prior art. The ID concluded that SK hynix showed that it would have been obvious to produce module control signals based on a set of address and control signals. Final ID at 119-23. The ID relied on the testimony of Dr. Subramanian, who testified that it would have been obvious to use a buffer with the QBM reference to produce control module signals based on a set of address and control signals. RX-2006C (Subramanian DWS) at Q/A 1049. Dr. Subramanian further testified it would have been obvious to combine the QBM

prior art with a rank multiplication configuration, which involves using both a chip-select and a decoded address signal to increase memory space, and thus produce a first module control signal in response to both input address and control signals. *Id.* He further testified that it would have been obvious to combine that QBM reference with module control functionality, which would result in the second module control signals for the QBM switches to be produced in response to both input address and control signals. *Id.* In other words, the ID relied upon evidence showing that it would have been obvious to produce each of the first and second module control signals in response to both input address and control signals, so the Commission’s modification to this construction of “produce...” does not change the ALJ’s invalidity result. Accordingly, the Commission affirms the ID’s finding that claims 1-5, 7, 8, 10, 14, and 15 of the ’907 patent are invalid as obvious in light of QBM based on the modified claim constructions set forth herein and for the reasons set forth above and in the Final ID.

C. Additional Grounds for Finding the Technical Prong of the Domestic Industry Requirement Not Satisfied with Respect to the ’907 Patent

As explained above, the Commission finds that Netlist failed to establish the technical prong of the domestic industry requirement as to the ’907 patent for the same reasons Netlist failed to establish infringement.⁸ In addition, for the reasons set forth below, the Commission determines that Netlist failed to establish the technical prong of the domestic industry requirement as to the ’907 patent by failing to analyze adequately its domestic industry product and present evidence on the actual functionality of its domestic industry products.

⁸ Netlist failed to establish the technical prong of the domestic industry requirement as to the ’623 patent. Netlist concedes that the technical prong with respect to that patent rises and falls with infringement, Final ID at 62, and Netlist did not petition for review of the Final ID’s finding that Netlist failed to establish infringement of the ’623 patent.

1. Overview

The ALJ found that the technical prong of the domestic industry requirement for the '907 patent rose and fell with his findings on infringement for the '907 patent. Final ID at 103-04. He found that SK hynix waived its challenge to the technical prong by not including that argument in its pre-hearing brief. *Id.* at 103. The ALJ also rejected OUII's argument that Netlist failed to carry its burden by failing to analyze the circuitry of the alleged domestic industry products, and instead found that Netlist's analysis of the JEDEC standard is sufficient to establish the technical prong by the preponderance of the evidence. *Id.*

2. The Parties' Arguments

Netlist argued that the alleged domestic industry products' compliance with JEDEC standards is sufficient to satisfy each and every limitation of the asserted claims of the '907 patent. Netlist Init. Sub. at 10-21. Netlist then argued that the evidence showed that each limitation was satisfied by reference to JEDEC standards, including by arguing that the domestic industry product satisfied the "do not receive" limitation because the memory device does not "acquire" data or perform the first stage of a write operation. *Id.* at 13-21.

SK hynix argued that, under its proposed constructions for "receive" and "produce," the '907 patent is not essential to any JEDEC standard, and thus Netlist's reliance on JEDEC standards is fundamentally insufficient to show infringement. SK hynix Init. Sub. at 14-15. SK hynix also argued that, under the ALJ's constructions, the Final ID found infringement of the "receive" / "do not receive" limitation based on the internal circuitry of the SK hynix memory device, but Netlist failed to present any such evidence of such internal circuitry for the domestic industry products. *Id.* at 16-22; SK hynix Rep. Sub. at 8-11.

OUII argued that Netlist's domestic industry argument is a baseless assertion that the accused products and domestic industry products are identical. OUII Rep. Sub. at 8-23. OUII

contended that compliance with JEDEC standards was insufficient to establish the technical prong of the domestic industry requirement because, while the accused products and domestic industry products use JEDEC-compliant components, there was no evidence that the collective implementation of these different components results in the accused and domestic industry products having identical relevant functionality. OUII Init. Sub. at 29-30. OUII further argued that Netlist's expert did not even have access to the domestic industry products' circuitry, and thus Netlist failed to present any evidence regarding the relevant circuitry of its domestic industry products. *Id.* at 30-31; OUII Rep. Sub. at 8-23.

3. Analysis

As an initial matter, the Commission found above that the JEDEC-compliant accused products do not infringe any asserted claims of the '907 patent, which shows that JEDEC-compliance does not necessarily require the practice of the claims of the '907 patent. Because Netlist relies solely on JEDEC compliance to show that its domestic industry products practice claims of the '907 patent, Netlist's technical prong argument fails for that reason alone.

But even if that were not the case, the Commission finds that Netlist failed to demonstrate the technical prong of the domestic industry requirement by failing to present any evidence on the actual functionality of its domestic industry products. The asserted claims of the '907 patent are highly detailed, and include, for example, a requirement that the "second memory devices do not output or receive any data associated with the memory read or write command." This limitation requires an absolute prohibition (*i.e.*, that the devices "do not output or receive") over a broad class of data (*i.e.*, "any data" that is even "associated with the memory read or write command"). Regardless of the meaning of "receive," the satisfaction of the above limitation requires an analysis of the entire memory device (or at least all of its inputs and outputs) to ensure that no data associated with the "command" is received or outputted by the memory

device.

Netlist failed to supply such an analysis. Netlist's expert, Dr. Levitt, relied solely upon the JEDEC DDR4 SDRAM specification's statement that the system will read or write to a first or second memory depending on whether the CS pin has a low or high value. CX-2003C at Q/A 659-61. But while the JEDEC standard describes how to select the first memory device, the JEDEC standard does not address whether the nonselected second memory device does or does not output or receive "any data associated with the memory read or write command," as required by the claims. In other words, Netlist's only evidence for the "do not output or receive" limitation is a JEDEC standard that does not even address whether the nonselected memory device outputs or receives the data. Accordingly, the Commission finds that Netlist failed to present any evidence that the accused products satisfy the limitation "the second memory devices do not output or receive any data associated with the memory read or write command."

Nor did Netlist elsewhere analyze the domestic industry products for this limitation. Netlist's entire technical prong argument in its post-hearing brief consisted of a single paragraph that concluded without explanation that the accused and domestic industry products are identical. Netlist Initial Post-Hearing Br. at 54. Although the claim language involves the memory device's receipt and output of signals, Netlist's only expert on the issue repeatedly testified that he never even looked at the circuitry of the memory devices in the domestic industry devices. Hearing Tr. (Levitt) at 431:13-432:9. Dr. Levitt contended that he did not need to analyze the circuitry because the domestic industry devices still needed to provide JEDEC-standard functionality, but he admitted that the relevant JEDEC standard is just a block diagram that does not dictate any specific circuit configuration. Hearing Tr. (Levitt) at 446:3-15. Moreover, as discussed above, Netlist's cited JEDEC standards are silent on whether the nonselected memory

devices receive or output “any data” as required by the claims, so Netlist needed to show that the domestic industry products had circuitry that satisfied the limitation. By failing to look at the actual circuitry of the memory devices, Dr. Levitt had no basis to conclude that the second memory device does not output or receive “any data associated with the memory read or write command.” Accordingly, the Commission finds no domestic industry on this independent basis.

D. The Economic Prong of the Domestic Industry Requirement as to the ’623 and the ’907 Patents

On review, the Commission has determined to take no position on whether Netlist satisfied the economic prong of the domestic industry requirement to both of the ’623 and ’907 patents.

E. The Requirement to Offer a License on “Reasonable and Non-Discriminatory” Terms

For the reasons set forth below, the Commission finds that the JEDEC Patent Policy was not shown to be unenforceable and that neither the ’907 patent nor the ’623 patent was shown to be essential to any JEDEC standard. The Commission discusses these findings below, reverses the Final ID’s determination that the JEDEC Patent Policy was shown to be unenforceable, reverses the Final ID’s determination that the ’907 patent was shown to be essential to a JEDEC standard, and vacates other findings on RAND in the Final ID.

1. Enforceability

a. Overview

Pursuant to the JEDEC Manual and Patent Policy, Netlist and SK hynix agreed to provide licenses under reasonable and nondiscriminatory terms in certain circumstances. RX-2659 (JEDEC Manual). The Final ID found that the JEDEC Patent Policy agreement is unenforceable under New York contract law because the terms “reasonable” and “non-discriminatory” are ambiguous. *Id.* at 175-76.

b. Parties' Arguments

No party argued that the JEDEC Patent Policy is not enforceable.

c. Analysis

The Commission has determined to reverse the ID's finding that the JEDEC Patent Policy is unenforceable. The Final ID relied on *Cobble Hill Nursing Home, Inc. v. Henry and Warren Corp.*, which stated that "before rejecting an agreement as indefinite, a court must be satisfied that the agreement cannot be rendered reasonably certain by reference to an extrinsic standard that makes its meaning clear," such as "reference to an extrinsic event, commercial practice or trade usage." 548 N.E.2d 203, 206 (N.Y. 1989). The Commission finds that the ALJ erred by not assessing whether the frequent use of "reasonable and nondiscriminatory" terms by standard-setting organizations shows that the phrase is reasonably certain in commercial practice or trade usage, particularly in light of the numerous court cases that have found such agreements enforceable. *See, e.g., TCL Commc'n Tech. Holdings, Ltd. v. Telefonaktiebolaget LM Ericsson*, 2018 WL 4488286 (C.D. Cal. Sept. 14, 2018).⁹ The use of these terms by numerous standard-setting organizations in similar agreements and the decisions of courts to interpret the provisions suggests that this agreement is enforceable, especially in light of *Cobble Hill's* holding that a contract should be declared unenforceable only as "a last resort." 548 N.E.2d at 206.

Accordingly, the Commission finds that the record does not demonstrate that the JEDEC Patent Policy is unenforceable under New York law, and therefore reverses the ID's finding that it is unenforceable.

⁹ *See also, e.g., Microsoft Corp. v. Motorola, Inc.*, 696 F.3d 872, 884-85 (9th Cir. 2012); *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, Case No. 6:18-cv-00243-JRG, 2019 WL 4734950 (E.D. Tex. May. 22, 2019); *Realtek Semiconductor Corp. v. LSI Corp.*, 946 F. Supp. 2d 998, 1005-08 (N.D. Cal. 2013); *Apple, Inc. v. Motorola Mobility, Inc.*, 886 F. Supp. 2d 1061, 1083-87 (W.D. Wis. 2012).

2. Essentiality

a. Overview

The ID made a contingent finding on essentiality, stating that “if the Commission determines that the ’907 patent is infringed in this Investigation, the undersigned finds that the evidence of record would support the conclusion that the Asserted Claims of the ’907 patent are essential to a JEDEC standard.” *Id.* at 175. Under that reasoning, the Final ID concluded that the ’907 patent is essential because it found infringement of two of the ’907 patent claims, and that the ’623 patent is not essential because its claims are not infringed. *Id.* at 174-175.

b. Parties’ Arguments

Netlist argued that the asserted claims of the ’907 patent are essential to the JEDEC DDR4 LRDIMM standard based on: (1) Netlist’s commitment of the ’907 patent as essential to the JEDEC DD4 LRDIMM standard; (2) Netlist’s adherence to JEDEC policy governing essential patent claims; (3) Netlist’s steadfast contention that the asserted claims are essential; and (4) the Final ID’s finding that the admittedly-DDR4-JEDEC-compliant accused products infringed the asserted claims of the ’907 patent. Netlist Initial Sub. at 8-10.

SK hynix argued that, under the proper construction for “receive” and/or “produce . . .”, the ’907 patent is not essential to any JEDEC standard. SK hynix Init. Sub. at 12-13. SK hynix, however, argued that, if the Commission rejects SK hynix’s arguments and finds a violation, then the ’907 patent is essential to a JEDEC standard based on Netlist’s binding admissions. *Id.* at 13-14.

OUII argued that there is no evidence in the record showing that the ’907 patent is essential to any JEDEC standard. OUII Init. Sub. at 22-29. OUII contended that Netlist relied solely upon the JEDEC DDR4 standard for infringement, but failed to provide any evidence as to whether its cited portions of the DDR4 standard were mandatory or whether the accused

products actually used the cited functionality. *Id.* at 23-27. OUII further argued that SK hynix provided no evidence that compliance with any JEDEC standard necessarily infringes an asserted claim of the '907 patent. *Id.* at 28-29. In its reply brief, OUII pointed out that neither Netlist nor SK hynix identified any evidence that supports a finding of essentiality, and instead pointed to Netlist's mere representations that the patent is standard essential. *Id.* at 7.

c. Analysis

As an initial matter, the Commission finds the JEDEC-compliant accused products do not infringe either the '907 or '623 patent. Accordingly, Netlist failed to show that compliance with JEDEC standards would necessarily infringe the '907 or '623 patents, and therefore those patents are not shown to be essential to any JEDEC standard.

Regardless of that finding, the Commission finds that the Final ID's analysis is flawed. The Final ID concluded that, if a patent is infringed by a standard-compliant product, then the patent is essential to that standard. But under the JEDEC Patent Policy, a claim is essential to a JEDEC standard only if compliance with the required portions of the JEDEC standard would necessarily infringe the claim:

Essential Patent Claims: Those Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard.

NOTE Essential Patent Claims do not include Patent claims covering aspects that are not required to comply with a JEDEC Standard, or are required only for compliance with sections that are marked "example," "non-normative," or otherwise indicated as not being required for compliance, or related to underlying enabling technologies or manufacturing techniques not specified in the standard.

RX-2659 (JEDEC Manual) at .00030-31. Accordingly, to show standard essentiality, a party needs to show not only that the standard-compliant product infringes but also that compliance

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with the mandatory portions of the standard necessarily requires infringement. Because the Final ID did not address whether mandatory portions of the standard required infringement, the Final ID erred by finding essentiality.

The record shows that no party presented any evidence explaining why the asserted claims of the '907 patent or the '623 patent are essential to any JEDEC standard. Netlist purported to "admit" that its patents are standard-essential to bolster its infringement case, but provided no evidence or argument in support of that admission. SK hynix seeks to rely on Netlist's "admission," but SK hynix too provided no evidence or argument that the asserted claims of the '907 or '623 patents are standard essential. Indeed, at no point in their essentiality analyses did Netlist or SK hynix identify a specific patent claim or a specific JEDEC standard, let alone explain why the mandatory portions of that standard necessarily require the infringement of that patent claim. Accordingly, the Commission finds that neither the '907 patent nor the '623 patent are standard essential based on the lack of evidence regarding essentiality.

IV. CONCLUSION

For the foregoing reasons, the Commission finds that Netlist failed to establish a violation of section 337 by SK hynix.

By order of the Commission.

A handwritten signature in black ink, appearing to read "Lisa R. Barton", with a stylized flourish at the end.

Lisa R. Barton
Secretary to the Commission

Issued: April 21, 2020

**CERTAIN MEMORY MODULES AND COMPONENTS
THEREOF**

Inv. No. 337-TA-1089

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **COMMISSION OPINION** has been served by via EDIS the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on **April 21, 2020**.



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